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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				Application / C nt. N .	Unknown 10 / 2011
				Filing Date	November 12, 2003
				First Nam d Inv nt r	Kevin T. Look
				Art Unit	Unknown 281
				Examiner Name	Unknown
Sheet	1	of	2	Attorney Docket Number	X-1144 US

[illegible][illegible]

Examiner Signature	<i>Steve Ball</i>	Date Considered	7/19/05
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			Filing Date	November 12, 2003	
			First Named Inventor	Kevin T. Look	
			Art Unit	Unknown	
			Examiner Name	Unknown	
Sheet	2	of	2	Attorney Docket Number	X-1144 US

OTHER – NON PATENT LITERATURE DOCUMENTS				
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>	
SJT		TOYOJI YAMAMOTO et al., "Bias Temperature Instability in Scaled p+ Polysilicon Gate p-MOSFET's," IEEE Transactions on Electron Devices, Vol. 46, No. 5, May 1999, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997.		
SJT		N. KIMIZUKA et al., "NBTI enhancement by nitrogen incorporation into ultrathin gate oxide for 0.10-um gate CMOS generation," 2000 Symposium on VLSI Technology Digest of Technical Papers, April 2000, pp. 92-93, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997.		
SJT		JEROME B. LASKY et al., "Comparison of Transformation to Low-Resistivity Phase and Agglomeration of TiSi <sub>2</sub> and CoSi <sub>2</sub> ," IEEE Transactions on Electron Devices, Vol. 38, No. 2, February 1991, pp. 262-269, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997.		
SJT		SE-AUG JANG et al., "Effects of Thermal Processes After Silicidation on the Performance of TiSi <sub>2</sub> /Polysilicon Gate Device," IEEE Transactions on Electron Devices, Vol. 46, No. 12, December 1999, pp. 2353-2356, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997.		
SJT		MOHSEN ALAVI et al., A PROM Element Based on Salicide Agglomeration of Poly Fuses in a CMOS Logic Process, July 1997, pp. 855-858, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997.		
SJT		ALEXANDER KALNITZKY et al., "CoSi <sub>2</sub> integrated fuses on poly silicon for low voltage 0.18um CMOS applications, September 1999, pp. 765-768 IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997.		

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